

Adhesive wafer bonding using photosensitive polymer layers

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ABSTRACT

Adhesive wafer bonding is a technique that uses an intermediate layer for bonding (typically a polymer). The main advantages of using this approach are: low temperature processing (maximum temperatures below 400°C), surface planarization and tolerance to particles (the intermediate layer can incorporate particles with the diameter in the layer thickness range). Evaporated glass, polymers, spin-on glasses, resists and polyimides are some of the materials suitable for use as intermediate layers for bonding. The main properties of the dielectric materials required for a large field of versatile applications/designs can be summarized as: isotropic dielectric constants, good thermal stability, low CTE and Young's modulus, and a good adhesion to different substrates.

This paper reports on wafer-to-wafer adhesive bonding using SINR polymer materials. Substrate coating process as well as wafer bonding process parameters optimization was studied. Wafer bonds exceeding the yield strength of the SINR polymer were accomplished on 150 mm Si wafers. Features of as low as 15 µm were successfully resolved and bonded. A unique megasonic-enhanced development process of the patterned film using low cost solvent was established and proven to exceed standard development method performance. Statistical analysis methods were used to show repeatability and reliability of coating processes.

Keywords: adhesive wafer bonding, polymer bonding, MEMS, planarization, low temperature bonding, photosensitive

1. INTRODUCTION

Various wafer bonding processes are used in medium and large volume production of Micro-Electro-Mechanical Systems – MEMS (e.g. accelerometers, gyroscopes), Silicon-on-Insulator (SOI) substrates, consumer products and advanced substrates (e.g. Germanium-on-Insulator: GOI, Strained Silicon-on-Insulator: SSOI, etc.).

In order to expand the field of applications, there is a high interest in developing low temperature wafer bonding processes. In wafer bonding the temperature limit for low temperature range is about 400°C. The thermal annealing step can be considered the main limitation of wafer bonding, as the thermal mismatch of the two substrates to be bonded will always result in high stress built-in at the bonded interface. The effect of the thermally induced stress is usually a high bow of the bonded pair (depending on materials, bow can go up to millimeters range for 100mm diameter wafers) or wafer breakage.

Some of the main advantages of wafer bonding which makes it valuable for MEMS applications are:
- process is not restricted to a certain type of substrate (applicable to semiconductors, metals, glass, polymers, etc.);
- if bonding partners are single-crystalline, their lattices do not have to match (as in case of epitaxy) but only their surfaces have to meet the requirements in terms of flatness, smoothness and cleanliness;
- this process is applicable at wafer level (depending on materials, up to 300 mm wafers), which gives an increased efficiency to manufacturing processes and opens new horizons in processes with high costs (e.g. moving from chip-level packaging to wafer level packaging in MEMS). Various principles are governing wafer bonding processes (fig. 1).

Among the different types, adhesive wafer bonding using polymer materials as bonding layers is of high importance due to some specific benefits:

- Compensation of surface defects: if wafer bonding is used to join patterned wafers there is a risk of generating surface defects during wafer preparation (e.g. scratches, local high roughness)
- Compensation of particles contamination: small amounts of particles remaining on the surface can be incorporated in the bonding layer if particle diameter is smaller than layer thickness.
- Low processing temperature compared to fusion bonding

- Relatively simple process flow (typically a standard sol-gel process: ambient conditions spin-/spray-coating followed by baking) compared with other thin film deposition methods requiring vacuum deposition (e.g. evaporation, sputtering).

Various types of polymer materials were reported being used as bonding layers [1-3]. Independent from the polymer class from wafer bonding perspective there are two main categories of polymer materials based on their behavior during bonding: one is represented by materials which become viscous and flow during bonding process while the second category is formed by materials which remain rigid after baking process and subsequently during bonding.

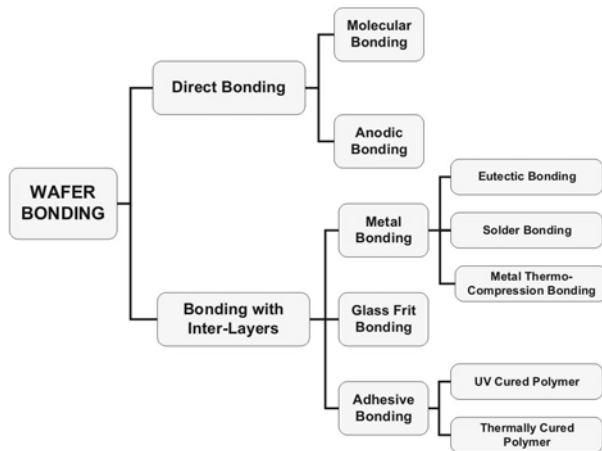


Fig. 1. Wafer bonding types.

The two different behaviors are very important for wafer bonding due to their major impact on process results. A “flow-able” polymer would offer the advantage of very good planarization of surfaces with high topography, while the major drawbacks are the risk of tooling contamination by material squeezing, and the lower wafer-to-wafer alignment accuracy due to bonding layer compression and high potential of shifting the substrates. A “rigid” polymer would bring the benefits of allowing high wafer-to-wafer alignment accuracy, of being able to maintain defined distances between the two substrates and subsequently the possibility to define patterns in the bonding layer just by photolithography (e.g. spacers, channels, etc.).

Polymer Young’s modulus becomes also a very important property when bonding substrates with different thermal expansion coefficients. In such applications low Young’s modulus polymers have the ability to absorb an important amount of thermally induced stress created during bond process, resulting in a low bow of the bonded substrates.

This work presents results on the use of a low modulus, low-k, negative-tone resist-type polymer material for adhesive wafer bonding.

2. EXPERIMENTAL

The process described in this paper is based on the use of a commercially available SINR™ material from Shin-Etsu MicroSi as bonding layer.

Table 1 is listing the main material parameters of the SINR™ polymer materials.

Table 1. SINR™ resist main features [4].

Chemistry	Siloxane
UV sensitivity	i-line, negative tone
Developer	IPA or PGME
Curing	180°C/1 h or 160°C/2 h
Shrinkage	<10%
Dielectric constant	2.6 (1 GHz)
Young’s modulus (25°C)	150 MPa
Water absorption	<0.1%

The experiments described in this paper were using a spin-on material (dry film also available). The schematic process flow is shown in fig. 2.

Si-wafers, 150mm diameter, (100)-oriented were used for tests. Spin-on deposition and baking were performed on an EVG®150 automated spin-/spray-coating equipment.

A randomized 12 experiment single factor DOE including 3 replicates was used for determining the spin-speed curve. Spin-coating process doesn't require the use of an adhesion promoter and consisted of dynamic dispense of the liquid SINR on the wafer and spinning the substrate at high rotation speed for obtaining the bonding layer. In order to check the thickness range for the used material four spin-drying speeds were used (2000 – 5000 rpm, in 1000 rpm increments) and for each condition (process flow: spin-coating, soft baking at 100°C followed by thickness measurement) were processed three samples.

To optimize film uniformity a non-replicated fractional factorial analyzing main effects and two factor interactions in 2 blocks was performed. A total of eight spin coat parameters with two levels were investigated. The experiment response variables were layer thickness and uniformity. Layer thickness was measured after a soft bake (100°C/1 min). Confirmation runs were completed after analysis of experimental data. ANOVA methods and residual analysis was performed on experimental data.

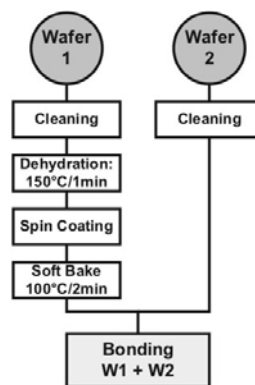


Fig. 2. Schematic process flow of adhesive wafer bonding with SINR™ polymers.

Two types of bonding layers were used for bond tests: blank and patterned. For the patterned layers preparation substrates coated with SINR™ material were exposed with UV in an EVG®620 mask aligner (dose: 1500 mJ/cm²) using a test mask containing different patterns with known dimensions. Two types of development processes were used for efficiency comparison: puddle development and megasonic-enhanced development.

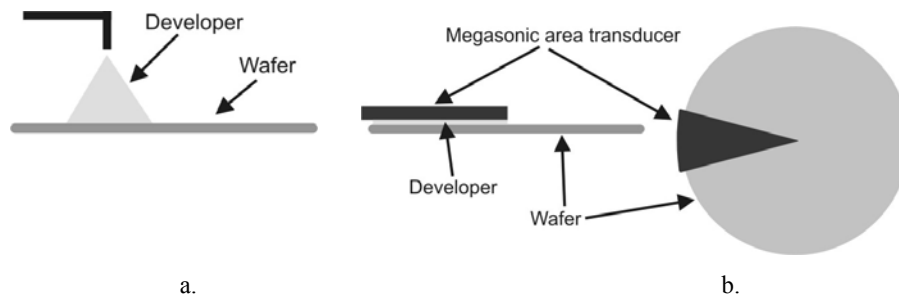


Fig. 3. Schematic drawing showing puddle development principle (a), and megasonic-enhanced development principle (b).

For puddle development the developer solution is sprayed onto substrate surface, left there for specified times and then spun off rinsed with isopropanol (fig. 3a). In the megasonic-enhanced development process a large area triangular-shape megasonic transducer providing high radial uniformity [5] is placed in close proximity to the wafer (in millimeter range) and a developer layer is maintained between the resist surface and the transducer surface.

The pattern features were investigated by optical microscope. Feature dimensions were labeled on the test mask and transferred to the polymer together with the line pattern.

After soft baking, one coated wafer and one bare Si wafer (only native oxide covered) were bonded together. The bond process was performed in an EVG® 520IS semi-automated bonder. A schematic drawing showing bond chamber setup is shown in fig. 4.

Wafers were loaded to the bond chuck (not shown in fig. 4) separated by three spacers and then the bond chuck was loaded to the bond chamber. The chamber was evacuated down to a vacuum range of 10^{-3} mbar and spacers were pulled out in vacuum in order to avoid trapping air between the two surfaces.

The two wafers in contact were uniformly heated simultaneously from bottom and top heaters and contact force was applied to press the two wafers together. The contact force is applied through the entire surface of top heater, which is mounted on a piston-like structure.

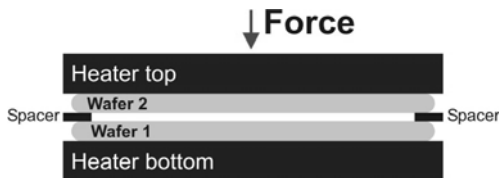


Fig. 4. Schematic drawing of bond chamber setup.

The bonding temperature was 180°C and three different bonding contact forces were tested (5000 N, 10000 N and 15000N). Bond tests were performed for both blank as well as for patterned polymer bonding layers.

After wafer bonding step the bonded interface quality was investigated by Scanning Acoustic Microscopy (SAM) using SONIX UHR-2001 equipment.

3. RESULTS AND DISCUSSION

Three wafers were spin-coated for each spinning speed, layer thickness was measured across the wafer and thickness uniformity was calculated. The obtained layer thickness was in the range 3.8 – 5.3 μm with a layer uniformity better than 4% (fig. 5). Such values recommend the polymer layers for wafer bonding.

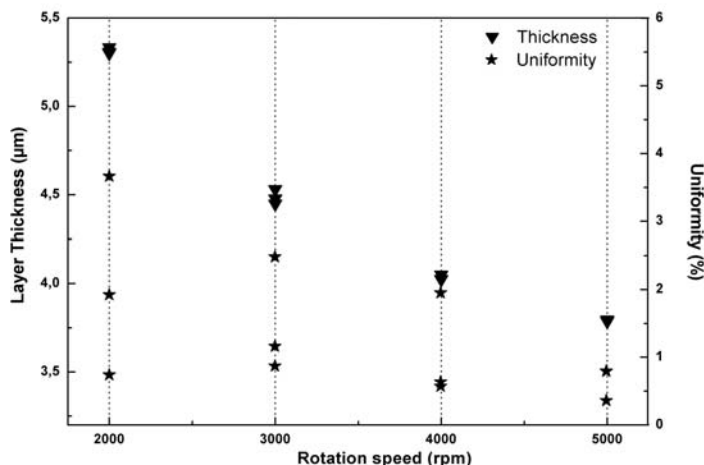


Fig. 5. Layer thickness and thickness uniformity vs. rotation speed for spin coated SINR layers.

Fig. 5 shows the layer thickness and uniformity vs. spin speed. The good thickness reproducibility for same spinning conditions (all three values for each spin speed are very close) correlated to the layer uniformity values, show a highly reliable spin-coating process.

A standard coating method resulted in well defined and reproducible spin speed curves. For further optimization and improved understanding of coating parameters and dynamics a factorial DOE was performed and analyzed. Figure 6 shows the analysis of variance with film uniformity as the response variable. The ANOVA proves the dispense spin speed for dynamic dispense, spin off speed, and coating chamber lid position (open/close) to be statistically significant at the 10 % significance level (p-value <0.1). Residual analysis of the randomized experiment does not show any run order effects. The normality graph proves the normal distribution of the response variable. The normal distribution is the key assumption and must be met in order for the statistical analysis to be accurate.

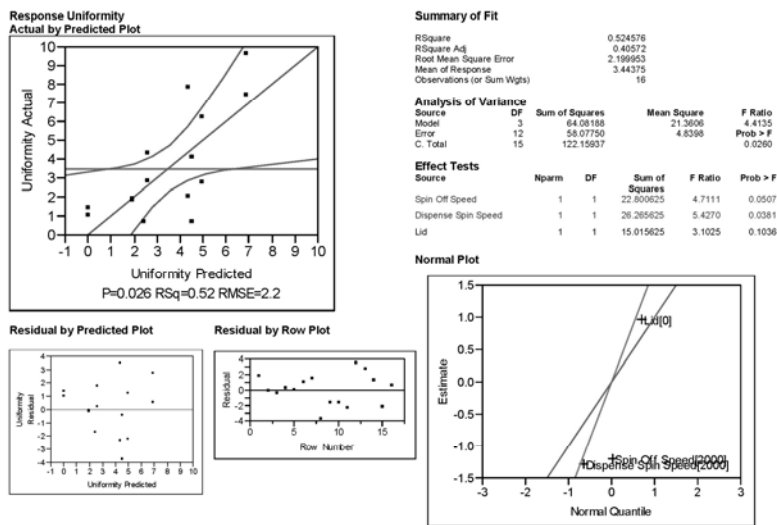


Fig. 6. Analysis of variance of spin coat variables with layer uniformity as the response variable.

For some of the test wafers polymer bond layers were patterned by direct photolithography. A test mask with known feature sizes was used for patterning. The test mask consisted of alternative bright field/dark field areas, each area containing line patterns. The polymer layers were prepared as described above for spin curve study and soft baked material was exposed in a mask aligner. For the first tests the polymer thickness (5 μm) and UV exposure condition (1500 mJ/cm²) were maintained constant and development conditions were varied in order to check the impact of the two processes on pattern quality.

In a first approach the development process efficiency was evaluated by using development times of 30 sec and 60 sec. After a rinse and pattern investigation with an optical microscope the development was continued by using additional 30 sec or 60 sec steps.

Megasonic-enhanced development was reported in literature as a possibility to improve line definition in fine pattern lithography (e.g. Electron Beam Lithography, [6]) for high aspect ratio features (sub-micrometer range). In the current work megasonic development was studied as a potential technique to improve pattern definition in a shorter time compared to puddle development. In the approach used for the current tests, the megasonic area transducer triangular shape ensures good uniformity of the acoustic energy across the entire developed surface.

Both the dark field as well as the bright field exposure modes were investigated as the test mask used offered this possibility. Table 2 summarizes the results of the development process for bright field exposure and table 3 shows results for dark field areas exposure. The features dimensions which were considered for evaluation of development efficiency for this set of experiments were ranging from 15 μm to 50 μm. In tables 2 and 3 the “+” sign means feature was resolved (well developed) while the “-” sign shows features which couldn’t be resolved by specific process condition.

Table 2. Development results (bright field).

Run no.	Development method	Process type (n x sec)	Total development time (sec)	Feature size				
				50 μm	40 μm	30 μm	20 μm	15 μm
1	Puddle	1x60	60	+	+	-	-	-
2	Puddle	2x60	120	+	+	+	-	-
3	Puddle	3x60	180	+	+	+	-	-
4	Puddle	4x60	240	+	+	-	-	-
5	Puddle	3x30	90	+	+	+	-	-
6	Megasonic	1x60	60	+	+	+	+	-
7	Megasonic	2x60	120	+	+	+	+	-
8	Megasonic	3x60	180	+	+	+	+	+
9	Megasonic	4x60	240	+	+	+	+	+
10	Megasonic	3x30	90	+	+	+	+	+

Table 3. Development results (dark field).

Run no.	Development method	Process type (n x sec)	Total development time (sec)	Feature size				
				50 μm	40 μm	30 μm	20 μm	15 μm
1	Puddle	1x60	60	-	-	-	-	-
2	Puddle	2x60	120	-	-	-	-	-
3	Puddle	3x60	180	+	+	-	-	-
4	Puddle	4x60	240	+	+	-	-	-
5	Puddle	3x30	90	+	+	-	-	-
6	Megasonic	1x60	60	+	+	+	-	-
7	Megasonic	2x60	120	+	+	+	+	-
8	Megasonic	3x60	180	+	+	+	+	-
9	Megasonic	4x60	240	+	+	+	+	+
10	Megasonic	3x30	90	+	+	+	+	-

Megasonic-enhanced development was able to resolve features as low as 15 μm while the minimum feature size resolved after puddle development for identical UV exposure and similar development time was 30 μm (bright field) or 40 μm (dark field). Examples of developed features are presented in fig. 7 (megasonic-enhanced development) and fig. 8 (puddle development).

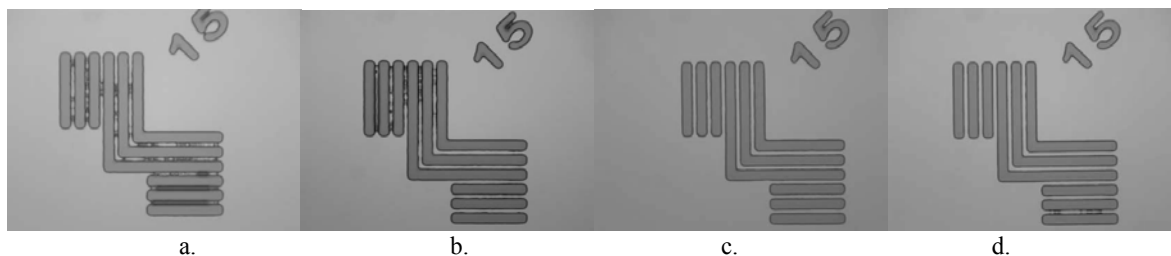


Fig. 7. Megasonic-enhanced developed 15 μm features for various time values (bright field): a. 1x60 sec, b. 2x60 sec, c. 3x60sec, and d. 3x30 sec.

In fig. 7 can be observed the improvement of feature shape with increasing the development time. Fig. 8 presents features developed using puddle development method. Compared to megasonic-enhanced development results the 15 μm features couldn't be resolved by puddle development at same process time. Higher iterations help reducing the development time for puddle development (features of 30 μm size could be resolved in 3x30 sec or 2x60 sec) but would not make a major difference in terms of development quality in case of megasonic-enhanced development as cavitation effect contributes to developer solution refreshing at the resist/developer interface.

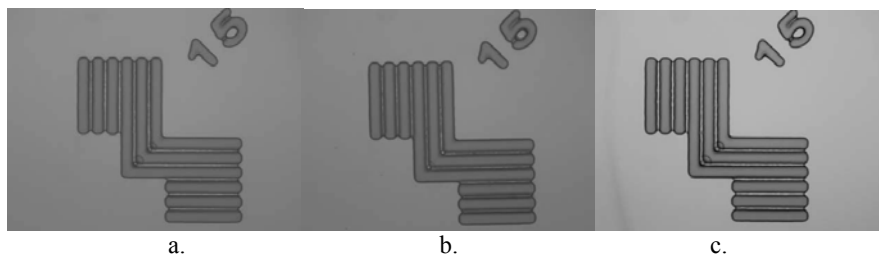


Fig. 8. Puddle developed 15 μm features for various time values (bright field): a. 2x60 sec, b. 3x60 sec, and c. 3x30 sec.

A first bond test was performed in order to check bonding suitability of the coated wafer. For this test wafers prepared as described in section 2 were bonded using the schematic process flow shown in fig. 2. In fig. 9 is presented an SAM image of a bonded wafer pair.

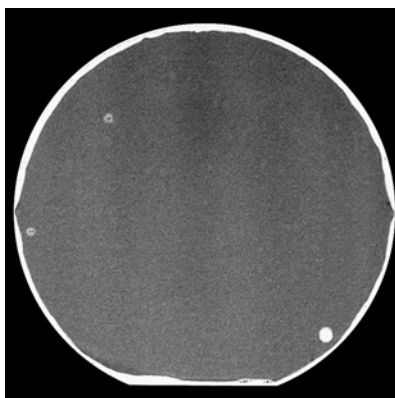


Fig. 9. Scanning Acoustic Microscope (SAM) image of a Si/Si pair bonded with SINR™ material.

The white edge ring was caused by an edge bead resulted from the spin coating process. This effect may impact on the bonding quality at wafer edge. In order to solve this problem it was decided to perform an edge bead removal after spin-coating process for each processed wafer. The three spots visible in fig. 9 were caused most likely by particles deposited on the coated surface during wafer handling after coating process (visual inspection of SINR™ layer after coating process didn't show any particles on the surface). Additional megasonic cleaning with deionized water was introduced to the process flow between coating and wafer bonding steps in order to prevent eventual airborne particles from sticking to the bonding layer surface.

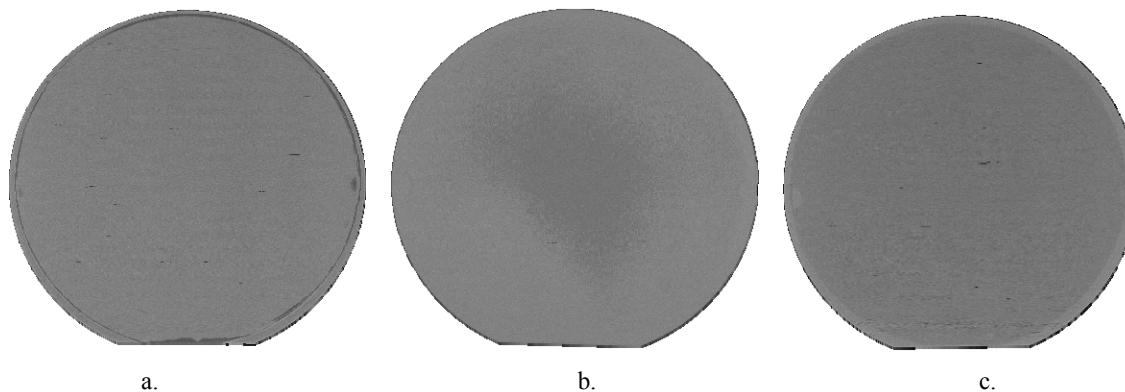


Fig. 10. SAM images of three Si/Si wafer pairs bonded with SINR layers at different contact forces: a. 5kN, b. 10kN, and c. 15kN.

Wafer bonding process was performed at three different contact forces keeping the same bonding layer preparation and wafer bonding temperature. Fig. 10 shows the SAM images of three samples bonded with different contact force values.

The light gray edge ring visible in all three images is due to edge bead removal after coating and the short white horizontal lines are an artifact of the inspection equipment and are not related to bonded interface quality.

It can be observed the interface quality is very good, just some small defects were observed at the edge. These defects were probably due to coating defects or due to the manual handling of wafers using tweezers.

Qualitative tests showed good adhesion of the polymer on both Si substrates (bond strength): when a blade is introduced at the bonded interface in order to try separating the substrates typically the polymer breaks and there is no delamination from the coated or from the bonded surface. There was no clear correlation between the specimen behavior during the blade test and the contact force value used for the bonding process.

Patterned polymer layers were also used for wafer bonding tests. Test wafers with bonding layers prepared as described at the beginning of this section were bonded to blank Si wafers using same process conditions as described above. In fig. 11 is presented the SAM image of a Si/Si wafer pair bonded through a patterned polymer layer.

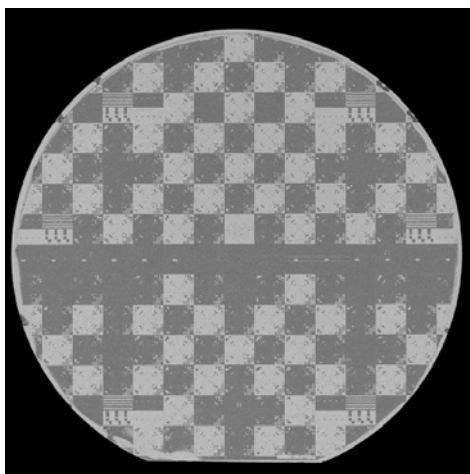


Fig. 11. SAM image of a 150 mm diameter Si/Si wafers pair bonded using a patterned SINR™ polymer bonding layer.

Detailed scans of the two types of bonded areas (realized by bright/dark field exposure) show good quality bonding even for the smallest size line features (fig. 12).

In fig. 12 can be observed that the polymer lines in the bright field areas are bonded without any shape distortion so there was no stress during bond process which may affect the pattern shape. The investigation of the smallest size bonded feature in the bright field areas (left side in fig 12a and 12b) is limited by the SAM lateral resolution, which for the particular equipment used was 5 μm .

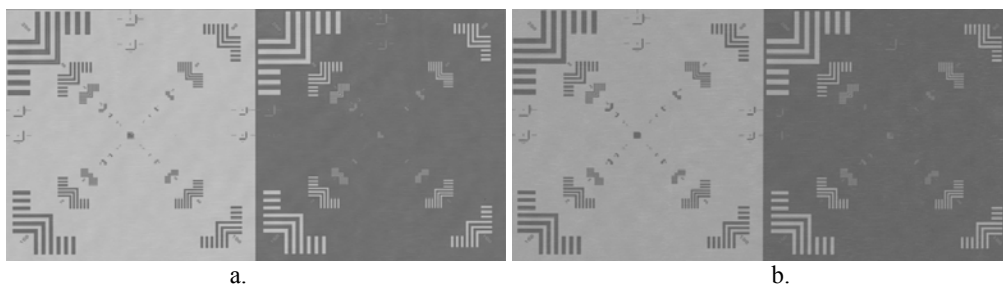


Fig. 12. Detail SAM image of the bright field (left side) and dark field (right side) areas for the bonded pair shown in fig. 12 taken for two different lateral scan resolutions: a.- 5 μm , and b.- 10 μm .

4. CONCLUSION

The use of various polymer materials as bonding layers for wafer bonding in MEMS applications was reported in literature during last years. This paper reports on feasibility of an adhesive wafer bonding process using SINRTM polymer bonding layers.

The most attractive features of this material for wafer bonding applications are the simple coating process (no adhesion promoter required), the low processing temperature (<200°C), the possibility to be directly patterned by photolithography, the low Young’s modulus (150 MPa), and its dielectric properties. Its behavior during bond process recommends this material as suitable for applications requiring substrate planarization prior to bonding and well defined adhesive layer thickness.

Wafer bonding applications considered for this process are dissimilar substrates bonding (low temperature wafer bonding and low Young’s modulus benefit), bonds with patterned layers (e.g. fluidic structures) and bonds requiring well defined spacers at the bonded interface.

Substrate coating, polymer patterning and wafer bonding processes were developed. Very high uniformity bonding layers with thicknesses in the range 3.8 – 5.3µm were obtained. Edge bead was removed after the coating process in order to ensure good bonding quality in the edge vicinity.

Patterning was realized by direct exposure (negative tone resist material) and two development methods: standard puddle development and megasonic-enhanced development. For megasonic-enhanced development a large area transducer with triangular shape was used. This shape assures uniform acoustic energy distribution across the wafer and avoids damaging of fine structures. The cavitation effect contributes to developer solution circulation at the wafer surface and increases the process efficiency. Megasonic-enhanced development resulted in shorter process time, and using the same development time the resolved features size was much smaller compared to the puddle development.

Wafer bonding was performed at 180°C (relatively low temperature) and the use of different contact forces during bonding process didn’t produce significantly different results. Patterned layers were successfully used for bonding. The line patterns showed no breakage after bond process, showing good adhesion of polymer to both silicon substrates.

Ongoing work is to explore the expansion of the polymer bonding layers thickness range and bonding of patterned layers. Additional work is focusing on photolithography patterning of SINRTM materials.

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