Characterization of 100 Micron Thick Positive Photoresist on 300 mm Wafers

Warren W. Flack, Ha-Ai Nguyen
Ultratech, Inc.
San Jose, CA 95134

Elliott Capsuto
Shin-Etsu MicroSi, Inc.
Phoenix, AZ 85044

Kelly Abreau
STEAG Hamatech USA
Santa Clara, CA 95051

The widespread adoption of advanced packaging techniques is driven by device performance and chip form factor considerations. Flip chip packaging is currently growing at a thirty percent compound annual rate and it is expected that in the near future over sixty percent of all 300 mm wafers will be bumped. To ensure optimal productivity and cost of ownership it is imperative to provide lithographic equipment and materials that are optimized for these applications. Due to the constantly shrinking bump pitch, it is critical to show excellent CD uniformity across the entire 300 mm wafer surface for feature sizes as small as 70 μm.

Flip chip packaging as well as Nanotechnology (MEMS) applications frequently use one or more very thick photoresist layers for electroplating applications. The plating levels require a photosensitive polymer material capable of coating, exposing and electroplating with conventional equipment and standard ancillary process chemicals. Additionally the process times for coating, baking, exposure and development must be considered since these impacts the overall cost of ownership of the lithography cell. For thick photoresist layers the sidewall profile, plating resistance and postplating stripability are important characteristics.

This study will characterize a novel single coat, positive tone photoresist (ShinEtsu SIPR®7120-20) used in electroplating levels up to 100 μm thick on 300 mm wafers exposed with the Ultratech Spectrum 300e^2 stepper and coated and developed with a Steag Hamatech Modutrack system. Process capability is determined by analyzing photoresist film thickness uniformity and critical dimension (CD) control across the wafer. Basic photoresist characterization techniques such as cross sectional SEM analysis are used to establish lithographic capabilities. This study shows excellent adhesion to copper with no surface treatment and no photoresist popping during exposure or post exposure bake (PEB). High aspect ratio, lead-free, solder structures were then electroplated using the optimized photoresist process to demonstrate photoresist durability and stripability.

Key Words: advanced packaging, flip chip, thick photoresist, MEMS, lead-free solder bump, electroplating, process optimization, 300 mm wafers.

1.0 INTRODUCTION

The semiconductor manufacturing industry is using advanced packaging techniques to reduce cost and improve performance by replacing single chip wire bonding with bump bonding applications as the final step in chip manufacturing. The advanced packaging market is growing at a compound annual rate of thirty percent as shown in Figure 1 [1]. The solder bump area is the largest component of this market. Today there is a rapid increase in the pin counts of most solder bump applications. The necessary corresponding reduction in bump pitch makes conventional “mushroom” type over plating impractical in high bump count devices as shown in Figure 2. Elimination of the umbrella requires even thicker photoresist layers since the entire solder volume is contained by the photoresist mold. Typical thicknesses for mushroom free processes are in the 60 to 100 μm range [2,3,4,5]. Extending the microlithographic processes into these rapidly growing areas is placing new demands on both the photosensitive materials and the lithography equipment.

Electroplating metals for micro-scale features is a well established technology. However, the fabrication of high aspect ratio linewidths for these applications is a new and challenging use of photolithography equipment and photoresists. The photolithography requirements for thick photoresists can be addressed by using optical lithography equipment similar to that developed for production of semiconductor devices. There are additional demands on the lithography process as bump processing extends to include 300 mm wafers. Coating thick photoresists on these larger size wafers is not trivial and posses many challenges. Thick photoresists typically require a high exposure dosage and a large depth of focus (DOF) for high aspect ratio lithography. For these reasons, it is advantageous to utilize a stepper with a broad band exposure system and low numerical aperture (NA) to maximize the illumination intensity at the wafer plane and to improve the DOF.

Photoresist performance, like stepper performance, has generally been optimized over recent years for achieving minimum geometries. Some newer photoresist formulations are available that have properties especially tailored for making the high aspect ratio structures required for electroplating molds. The process operating conditions for thick photoresists are considerably different than for thin photoresists. In the case of thin photoresists the two main issues are resolution and exposure latitude [6]. With thick films the concerns are centered around aspect ratios, downstream plating performance, exposure and focus latitudes and productivity. As spin coated photoresist films become more popular for these applications, it is important to study thick layers to determine how it might be optimized for performance and productivity [3,4,5] especially on 300 mm wafers.

Traditionally photoresists useful in the 50 μm to 100 μm range are very difficult to formulate, especially in a positive tone. Advantages of positive tone photoresists include, stripability, outgassing control, the ability to re-expose in the case of scumming, and compatibility with a dark field reticle [2,3,4,5]. It is very difficult to design a positive tone photoresist to achieve the necessary transparency, resulting in ultra-high exposure doses. Furthermore, very thick positive novalak photoresists have the characteristic of popping or void formation after exposure as a result of the nitrogen generated during exposure [4]. Productivity is also effected by the need to do multiple coats to achieve film thickness around 100 μm. For these reasons we investigated chemically amplified photoresists for this application. Chemically amplified photoresist do not show attributes of poor transparency, or voiding and 90 μm thickness in one coat. The objective of this study is to evaluate a positive tone, chemically amplified photoresist on 300 mm wafers. The experimental results include coating uniformity, CD linearity studies, plating performance, stripping performance and CD control.

2.0 EXPERIMENTAL METHODS

2.1 Lithography Equipment

Imaging of the SIPR 7120-20 photoresist was performed on an Ultratech Saturn Spectrum 300e^2 Wafer Stepper™. The optical specifications for the Saturn Spectrum 300e^2 are shown in Table 1. The stepper is based on the 1X Wynne-Dyson lens design employing Hg ghi-line illumination from 350 to 450 nm and having a 0.16 NA [7].

Broadband exposure is possible due to the unique design characteristics of the Wynne Dyson lens system. This symmetric catadioptric lens system does not introduce the chromatic aberrations common to other lens systems when broadband illumination is used. The low NA and broadband illumination spectrum of the Saturn Spectrum 300e^2 provide a more uniform aerial image through the depth of the ultra thick photosensitive materials in contrast to steppers with higher NA's and a relatively narrow bandwidth [5]. In addition, the Spectrum 300e^2 is equipped with a filter changer, which allows ghi-line (350 to 450 nm), gh-line (390 to 450 nm) or i-line (355 to 375 nm) illumination to be selected. This approach can be used to optimize lithographic performance based on the spectral sensitivity of the photosensitive material. The Spectrum 300e^2 stepper is configured to run both 300 mm and 200 mm wafer sizes. The stepper is also configured with a Wafer Edge Exposure (WEE) unit which uses a Hg arc lamp light source at the prealigner to expose the edge of the wafer. The purpose of the WEE features is to create a photoresist free area around the edge of the wafer for positive tone photoresists as a requirement at electroplating.

The photoresist for electroplating should be applied in a single coat to maximize throughput and therefore minimize the cost of ownership of the lithography cell. The coat and bake operations for this study were performed on Steag Hamatech Modutrack® equipment, which has precise control of spin speed and acceleration below 1000 rpm. The advanced spindle motor speed control supports precise acceleration to spread the photoresist uniformly to the edge of the wafer. A pump configured for high viscosity photoresist materials with large-diameter tubing facilitates the dispensing of high viscosity materials. To reduce particle defect density, a photoresist solvent is applied before the photoresist dispense through a dedicated line for pre-wet. A two-stage bake performed on separate hot plate modules was found to suppress micro-bubble formation during film drying. The low temperature first stage is used for a 80^{o}C bake for 3 minutes followed by the high temperature bake at 110^{o}C for 7 minutes, with a 0.2 mm proximity gap. Multiple bake modules can be configured using the modular stack bake feature, to allow increased throughput of these thick films.

The Ultratech 1X reticle used to characterize the process window was designed primarily to support cross sectional SEM metrology. This reticle consists of two fields of 10 mm by 10 mm, one of each polarity. Each field contains line and space patterns and square contact patterns from 10 µm to 100 µm. A second reticle was used for electroplating and has a 37 mm by 15.5 mm field size and contains 30 µm to 100 µm round contacts with various pitches.

Process characterization was performed using a focus/exposure pattern. Focus latitude of 70 µm contacts was determined by examining the cross section of square contact patterns with an Hitachi 7280-H SEM. Electroplating was done on another set of wafers exposed at best focus and best exposure using 96 exposure steps to completely cover the 300 mm wafer. The CDs were measured on a Joel JSM 6340F SEM and Boeckeler VIA-100 Video Measuring System before and after electroplating to check intra-wafer CD uniformity in conjunction with photoresist coating uniformity**.**

2.2 Photoresist Processing

SEMI standard 300 mm prime Cu seed wafers were used for this study. The photoresist used is Shin-Etsu SIPR 7120-20. The Shin-Etsu SIPR 7120-20 photoresist was coated with a a target thickness of 100 µm using the process and equipment described in Table 2. Photoresist thickness and uniformity were measured on a Dektak V300 profilometer.

Shin-Etsu SIPR 7120-20 photoresist is a TMAH developable, chemically amplified positive photoresist with high contrast and resolution. The nominal thickness at 3000 rpm is 20 µm which allows 100 µm thick coating in a single application. The viscosity of the photoresist is in the range of 5700 cps. The high viscosity is required to reach a 100 µm single layer coating. No HMDS was used as the adhesion of the photoresist was excellent on the substrates tested. TMAH 0.26N developer was used in the experiment. Even though this photoresist has only i-line sensitivity, it was not necessary to filter out the broadband wavelengths. The exposure wavelength is an inherent characteristic of a chemically amplified system depending on the choice of PAG (photo acid generator) materials. Post Exposure Bake (PEB) was required since the material is chemically amplified.

A second softbake was performed in a convection oven to ensure adequate removal of all solvents from the photoresist film. It has been shown that very rough sidewalls occur when the solvent is not removed completely [2]. A wait time from bake to exposure was required to complete the acid catalyzation process. However, it is possible to minimize the wait time by optimizing the bake time. The minimum delay time used for this study between coat and exposure and between exposure and development is one hour.

For electroplating, a second set of wafers were processed at nominal conditions (5800 mJ/cm^2 at -20 µm focus, ghi-exposure wavelength) using 96 exposure steps to completely cover the wafer. An edge exposure of 3 mm width was performed using the WEE to allow contact with the seed layer for electroplating. The electroplating processes are shown in Table 3. The photoresist can be easily stripped off by soaking in heated N-methyl pyrrolidone (NMP). No defects or plating bath contamination was reported. In addition a descum process was not used, however a standard chemical pre-clean was used before plating.

2.3 Data Analysis

After exposure the wafers were cleaved for cross sectional analysis on a Joel JSM 6340F, Hitachi S4100 or Hitachi 7280-H metrology SEM to show the CD linearity and depth of focus of square contacts. Top, middle and bottom CD measurements of the photoresist sidewall were taken at 1000X magnification for 70 µm square contacts. Only the middle CD measurements were used for the analysis in Section 3.0. Intra-wafer CD uniformity is illustrated using CD measurement of 70 µm contacts before and after plating.

3.0 RESULTS AND DISCUSSIONS

3.1 Baseline Photoresist Conditions

The process latitude of SIPR 7120-20 was evaluated using cross sectional SEM photographs of 70 μm square contacts in 90 μm thick photoresist on Cu seed substrates. Figures 3 (a) through (d) show exposure latitude with exposure dose variations from 5100 to 6000 mJ/cm^2 at a fixed -20 μm focus offset. At 5100 mJ/cm^2 (figure 3(a)) the sidewall is very straight with no noticeable foot. However, the CD is smaller than the reticle and there is a slight sidewall angle. At 5800 mJ/cm^2 (figure 3(c)) the CD is larger than the reticle and the sidewall flares slightly at the top of the photoresist. Therefore 5500 mJ/cm^2 was selected as the optimal exposure dose.

Figures 3 (e) through (h) show focus latitude through a focus variation from 0 to -40 μm at a fixed exposure dose of 5500 mJ/cm^2. At 0 μm focus offset (figure 3(e)) the sidewall has a significant slope and a noticeable foot at the bottom of the photoresist. At -40 μm focus offset (figure 3(h)) the sidewall flares slightly at the top of the photoresist. Therefore -20 μm focus was selected as the optimal focus.

3.2 Wafer Coating and Development

Photoresist thickness was measured at 160 locations evenly distributed over the 300 mm wafer to determine coating uniformity. A contour plot of the coating uniformity is shown in Figure 4(a). The solid contour lines represent 2.0 μm intervals and the dashed contour lines are half way between each solid line. There is a clear high region in the center of the wafer at 96 μm. The average thickness is 90.6 μm with a three sigma of 5.7 μm. This equates to a coating uniformity of 6.3 percent. This initial coating process was used in order to complete the solder electroplating in time to be included in this study. Subsequent enhancements to the coating process produced wafers with a three sigma of 2.8 μm as shown in Figure 4(b). The coating process enhancements are described in Table 4. The enhanced coating uniformity of 3.1 percent would have improved the final CD uniformity after electroplating if it had been available to be included in this study.

A set of 300 mm Cu seed wafers were exposed using the baseline process conditions discussed in section 3.1. Development was done in a batch mode using 0.26 normal TMAH at room temperature for 15 minutes. The photoresist cleared at around 9 minutes which implies the development time could have been reduced to improve throughput. No development time studies were performed for this study. After development the CD uniformity was measured a 30 locations evenly distributed over the wafer. A contour plot of the photoresist CD uniformity of 70 μm square contacts is shown in Figure 5(a). The solid contour lines represent 0.5 μm intervals and the dashed contour lines are half way between each solid line. The average CD is 68.6 μm with a three sigma of 3.2 μm. This equates to an across the wafer CD uniformity of 4.7 percent. The CD is smallest at center of the wafer with a size around 67 μm. A smaller CD would be expected since the photoresist is thicker at the center of the wafer as shown in Figure 4(a).

SEM photographs were used to determine the consistency of the photoresist slope and shape across the 300 mm wafer. Figure 5(b) shows cross sectional SEM photographs of 70 μm square contacts at five locations across the wafer (top, center, bottom, left, right). All of the locations show similar sidewalls and shape. It is apparent that the size is smallest in the center of the wafer and largest on the right side. This is consistent with the contour plot in Figure 5(a).

3.3 Electroplating

A set of 300 mm Cu seed wafers were exposed using the baseline process conditions discussed in section 3.1. The wafers were sent to Ebara Corporation for solder electroplating. No descum process was used, however a liquid preclean process was performed immediately before electroplating. After electroplating the wafers were stripped in heated NMP for 10 minutes, which compares favorably to the extremely long times required for many negative acting photoresists. The CD uniformity was measured a 35 locations evenly distributed over the wafer. A contour plot of the electroplated CD uniformity of the 70 μm round bumps is shown in Figure 6(a). The solid contour lines represent 1.0 μm intervals and the dashed contour lines are half way between each solid line. The average CD is 68.8 μm with a three sigma of 1.8 μm. This equates to an across the wafer CD uniformity of 2.6 percent. Again, the CD is smallest at the center of the wafer with a size around 68 μm. However, the contour plot has a less distinct ring pattern and the overall CD uniformity is better than that observed for the photoresist. The addition of a descum process would have also helped minimize even further the CD non-uniformity. The improved coating uniformity shown in Figure 4(b) would have helped improve CD uniformity even more. However the CD uniformity and CD size measured is more than adequate to meet future packaging requirements.

SEM photographs were used to determine the uniformity of the solder bump slope and shape across the 300 mm wafer. Figure 6(b) shows cross sectional SEM photographs of 70 μm round solder bumps at five locations across the wafer (top, center, bottom, left, right). All of the locations show similar sidewalls and shape. Plating height was measured on these five locations and averaged 89.9 μm with a total range of 4.5 μm for a height uniformity of 5.0 percent. Again the lowest point was in the center of the wafer. The addition of a descum process would have improved the plating height uniformity as well. Any residual photoresist on the surface of the open areas would have slowed the initiation of the plating. This possibly correlates with the thickest photoresist location in the center of the wafer.

3.4 Linearity

Cross sectional SEMs were used to determine the CD linearity of the photoresist and the shape of the final electroplated solder bump structures. Figures 7(a) through (d) shows square contacts from 100 to 50 μm in 100 μm thick photoresist on Cu seed substrates. The contacts were resolved down to 50 μm with similar sidewall profiles. The smaller contacts show slightly more flair at the top of the photoresist. Figures 7(e) through (h) shows round solder bumps from 100 to 50 μm that were electroplated from the same photoresist. A typical bump array for 60 μm solder bumps is shown in Figure 7(i). There is no indication of solder bridging between bumps. The bumps show excellent sidewall profiles with no signs of underbump plating. Clearly the photoresist demonstrated adequate durability in the electroplating bath with no cracking or adhesion failure. The Shin-Etsu 7120 photoresist used in conjunction with the equipment in this lithography cell exhibits solder bump fabrication capability that exceed current design requirements and offers the potential to meet future advanced packaging needs.

4.0 CONCLUSIONS

The objective of this study was to develop a process for a single coat, positive tone, 100 μm photoresist for bump processing on 300 mm wafers. In the past, formulating a positive tone, single coat, 100 μm photoresist has proven to be very difficult due to the high solids content. The SIPR 7120-20 was shown to meet these requirements. In addition standard novalak systems are not sufficient in regards to transparency so a chemically amplified system was used.

As expected, the switch to larger wafers sizes presented challenges not seen on smaller wafers. For example, developing an acceptable coating process in regards to thickness uniformity and defects was not trivial. It is not possible for to separate the photoresist performance from the plating performance in bump processes, so the investigation through electroplating is critical.

The SIPR 7120-20 photoresist performance easily meets requirements for both current and future generations of bump processing on 300 mm wafers using the Ultratech Spectrum 3e^2 and the Steag Hamatech Modutrack. This study demonstrated excellent resolution down to 50 μm, a good process window, and CD control of 3.2 μm (3σ) after plating for a 70 μm feature. Good single coat properties were obtained for films close to 100 μm thick. In addition, excellent plating performance was achieved along with an acceptable strip process. Also it should be noted that the resolution and CD control is more than sufficient to meet the needs of bump manufactures for future packaging requirements. Further follow up work was reported in this paper showing the improvements in coating uniformity which would also translate into improved CD control. Future work on the photoresist chemistry includes a faster version in order to improve throughput of the lithography cell. In conclusion, the photoresist material and the lithography cell equipment are available to support current and future production.

5.0 ACKNOWLEDGEMENTS

The authors would like to thank Mr. H. Kato, Mr. K. Toba and Mr. Hirano from Shin-Etsu Chemical for photoresist support and cross sectional SEM support. In addition, we would like to thank Dr. Kiumi Rei from Ebara for electroplating support as well as Hai Nguyen from Ultratech for photoresist process support.

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Parameter	Spectrum 300 e^2
Reduction factor	1X
Wavelength (nm)	350 - 450
Numerical aperture (NA)	0.16
Partial coherence (σ)	1.0
Wafer plane irradiance (mW/cm^2)	2250

Table 1: Optical specifications of the Saturn Spectrum 300e^2 stepper used in this study.

Process Step	Parameters	Equipment
SIPR 7120-20 Coat	PGMEA solvent pre-wet: 300rpm for 2 seconds Static dispense 19 ml quasi-static at 4 rpm Spread: 300 RPM for 1 second Spin: ramp to 775 RPM for 27 seconds	Steag Hamatech Modutrack
Softbake	Hotplate, 0.2 mm proximity 180 seconds at 80^{o}C 420 seconds at 110^{o}C	Steag Hamatech Modutrack
Oven Bake	120 minutes at 110^{o}C	Blue M oven
Exposure	Delay Time before exposure: 60 minutes ghi-line at 5800 mJ/cm^2, -20 μm focus, 3 mm WEE Delay Time after exposure: 30 minutes	Spectrum 300e^2
Post Exposure Bake	90 seconds at 95^{o}C	Steag Hamatech Modutrack
Develop	15 minute immersion in 2.38% TMAH, 21^{o}C Constant and aggressive agitation DI water rinse	

Table 2: Process conditions for Shin-Etsu SIPR 7120-20 for 100 μm thickness.

Process Step	Parameters	Equipment
Solder Electroplating	Lead-free Eutectic Sn-Ag Alloy 3.5 μm/minute, 25 ^{o}C	Ebara UFP-300M
Photoresist Stripping	NMP, 10 minutes at 60 ^{o}C IPA rinse, room temperature	

Table 3: Process conditions for lead free solder electroplating.

Process Step	Parameters	Equipment
SIPR 7120-20 Coat	PGMEA solvent pre-wet: 300rpm for 2 seconds Static dispense 19 ml quasi-static at 4 rpm Spread: 1200 RPM for 1.3 seconds at 4 krpm/sec Spread: 450 rpm for 5 seconds Dry: 175 rpm for 90 seconds Edge bead reduction: 1000 rpm for 1 second	Steag Hamatech Modutrack

Table 4: Enhanced photoresist coating process for Shin-Etsu SIPR 7120-20 for 100 μm thickness.

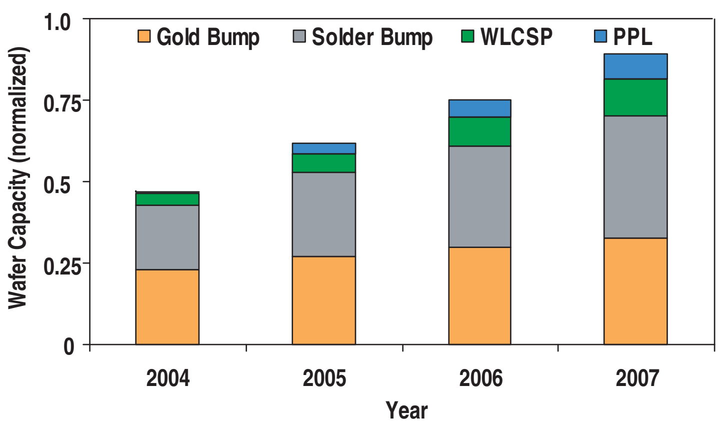

Figure 1: Wafer capacity forecast of 30% annual compound growth rate of the advanced packing market [8].

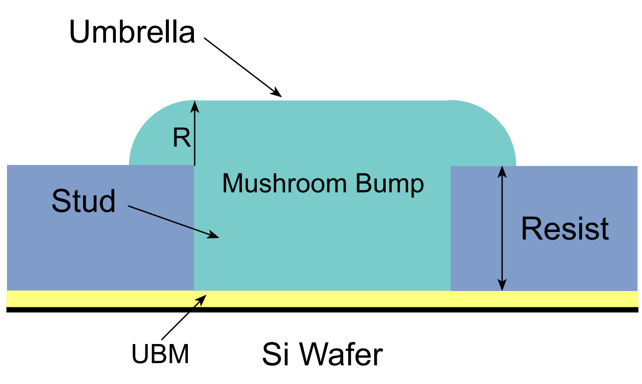

Figure 2: Cross section of a typical mushroom shaped bump. An ultra-thick photoresist allows sufficient solder volume buildup in the stud to eliminate the requirement for an umbrella.

Figure 3: SEM Photographs of process latitude of 70 μm square contacts in 100 μm thick ShinEtsu SIPR 7120, ghi-line exposure. The nominal condition is -20 μm focus and 5500 mJ/cm^2.

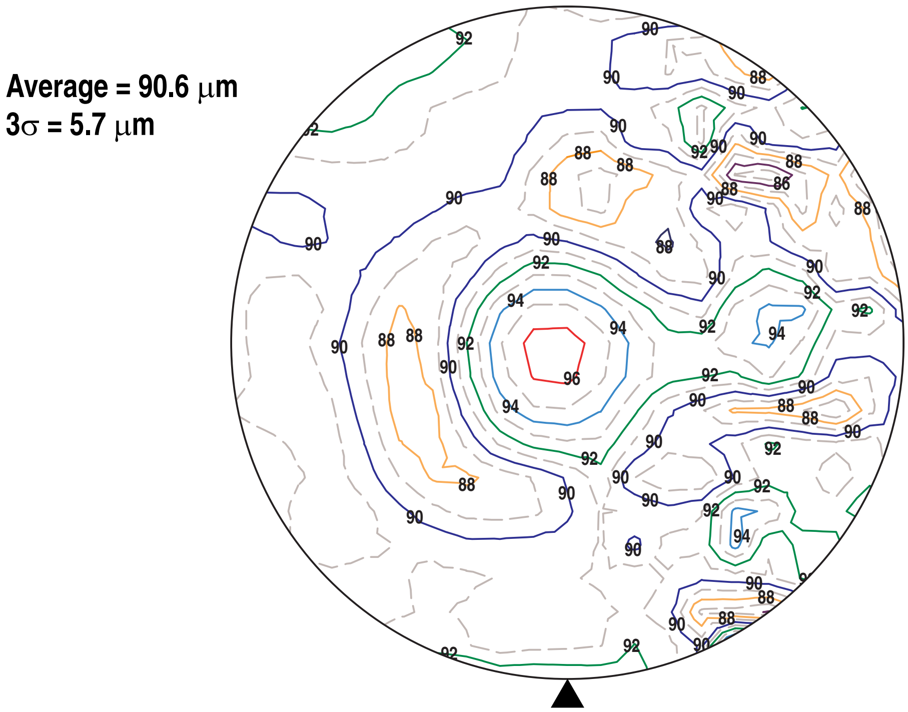

Figure 4(a): Coating uniformity for ShinEtsu SIPR 7120 on a 300 mm wafer after prebake. The solid contour lines are at 2.0 µm intervals and the dashed contour lines are half way between. This is the coating process used in this study.

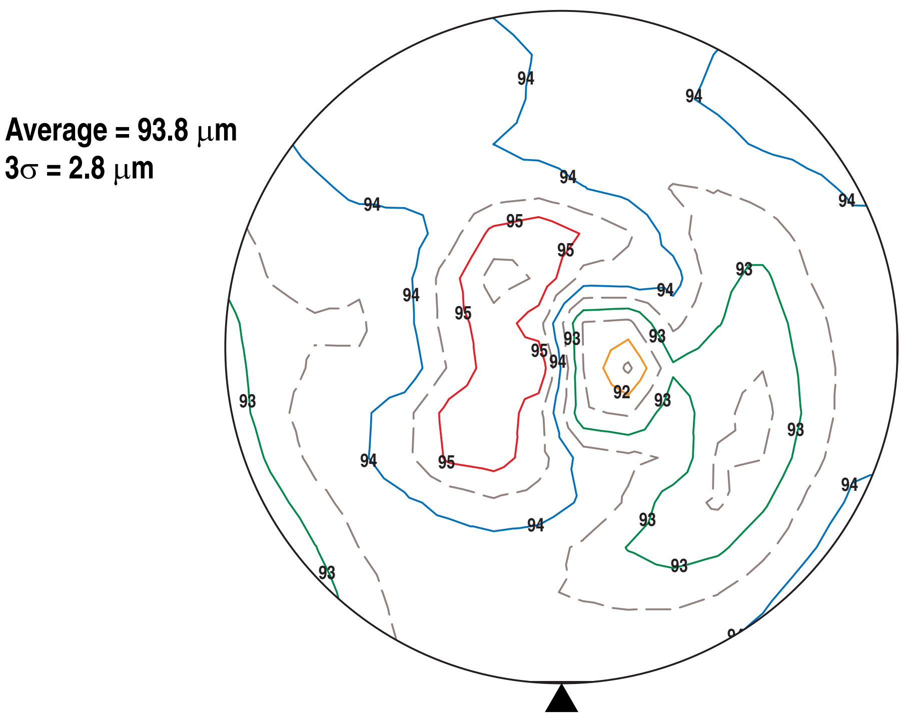

Figure 4(b): Enhanced coating uniformity for ShinEtsu SIPR 7120 on a 300 mm wafer after prebake. The solid contour lines are at 1.0 µm intervals and the dashed contour lines are half way between. This coating process was not available in time to be used in this study.

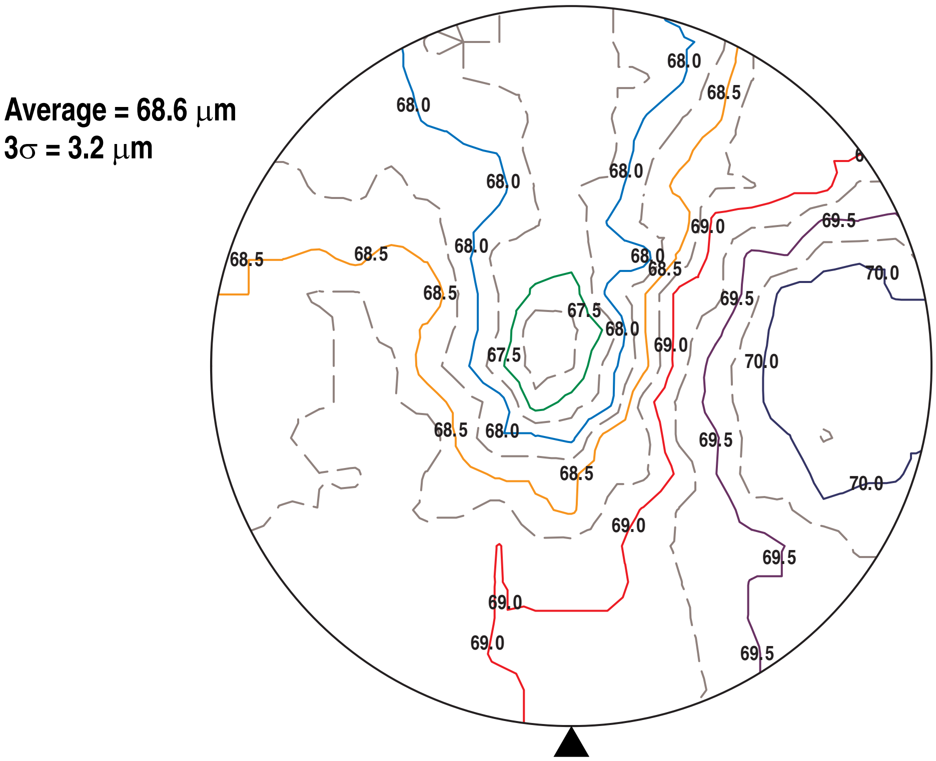

Figure 5(a): Photoresist CD uniformity of 70 μm square contacts in ShinEtsu SIPR 7120 on a 300 mm wafer. The solid contour lines are at 0.5 μm intervals and the dashed contour lines are half way between.

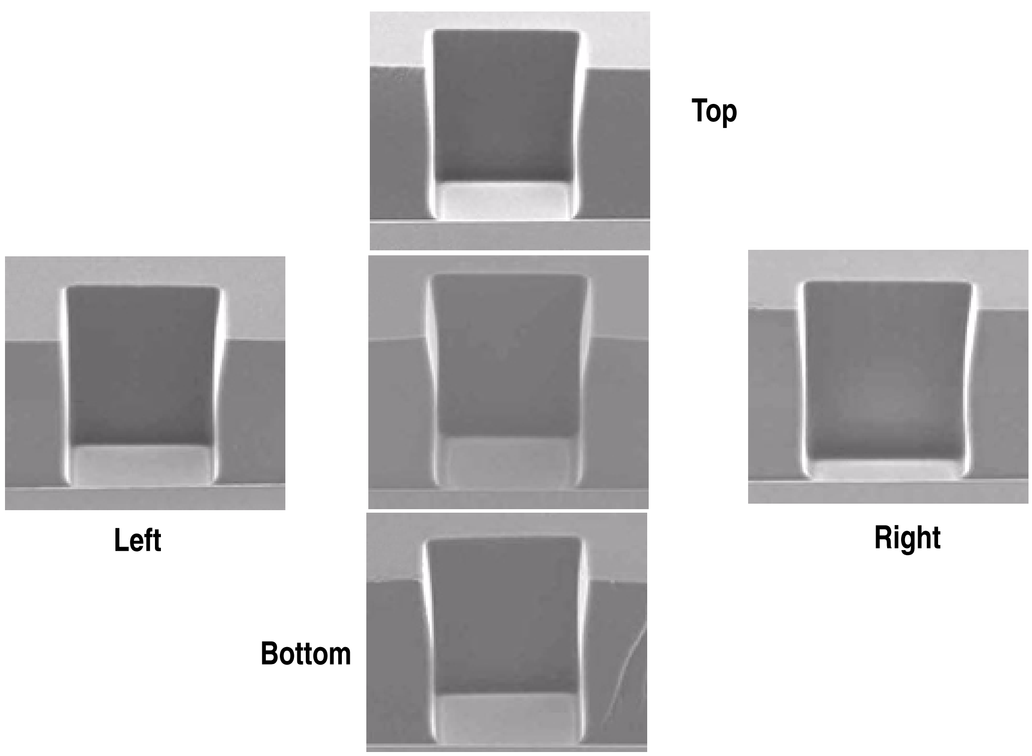

Figure 5(b): SEM Photographs of 70 μm square contacts in SIPR 7120 showing CD uniformity on a 300 mm wafer.

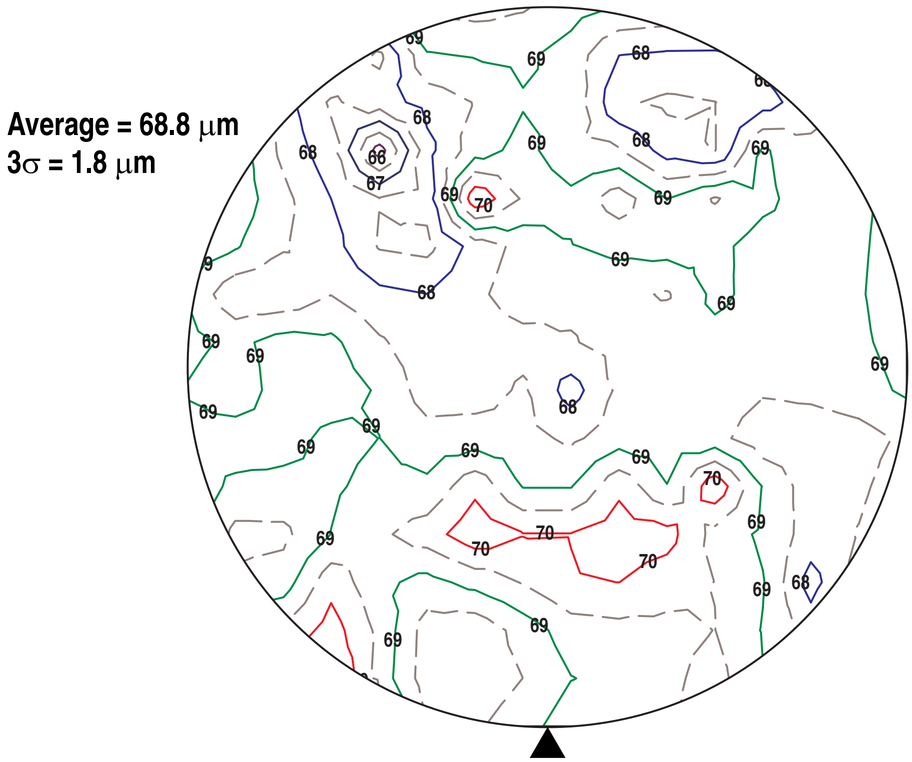

Figure 6(a): Electroplated CD uniformity of 70 µm solder bumps on a 300 mm wafer. The solid contour lines are at 1.0 µm intervals and the dashed contour lines are half way between.

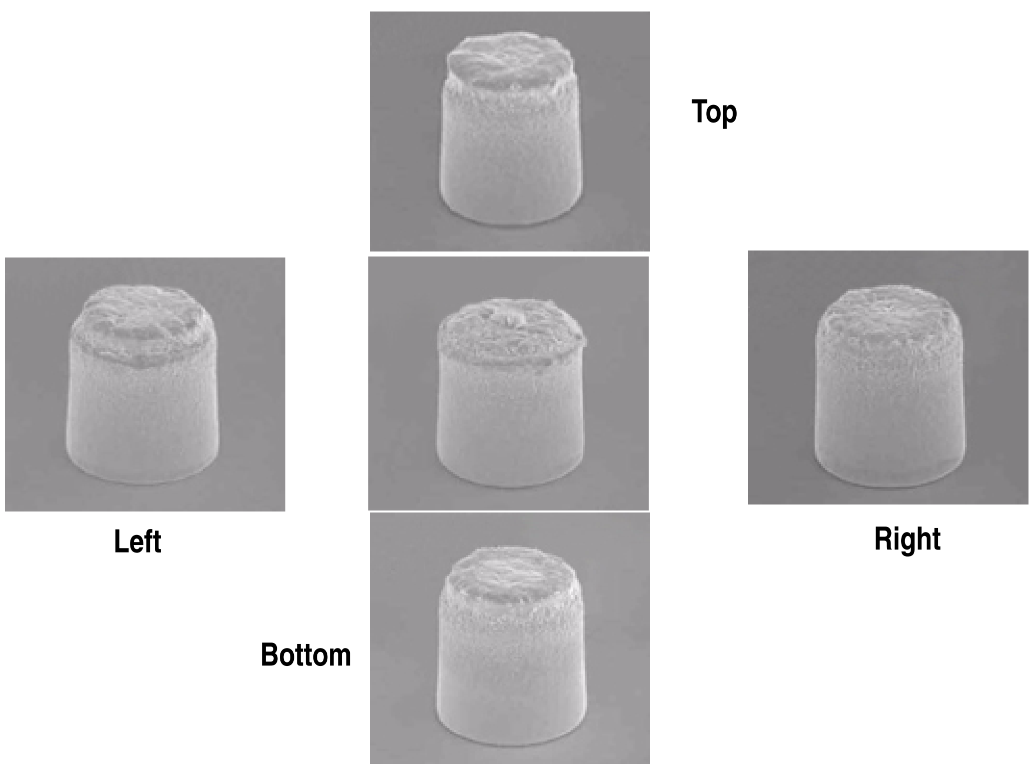

Figure 6(b): SEM Photographs of 70 µm electroplated solder bumps showing CD uniformity on a 300 mm wafer.

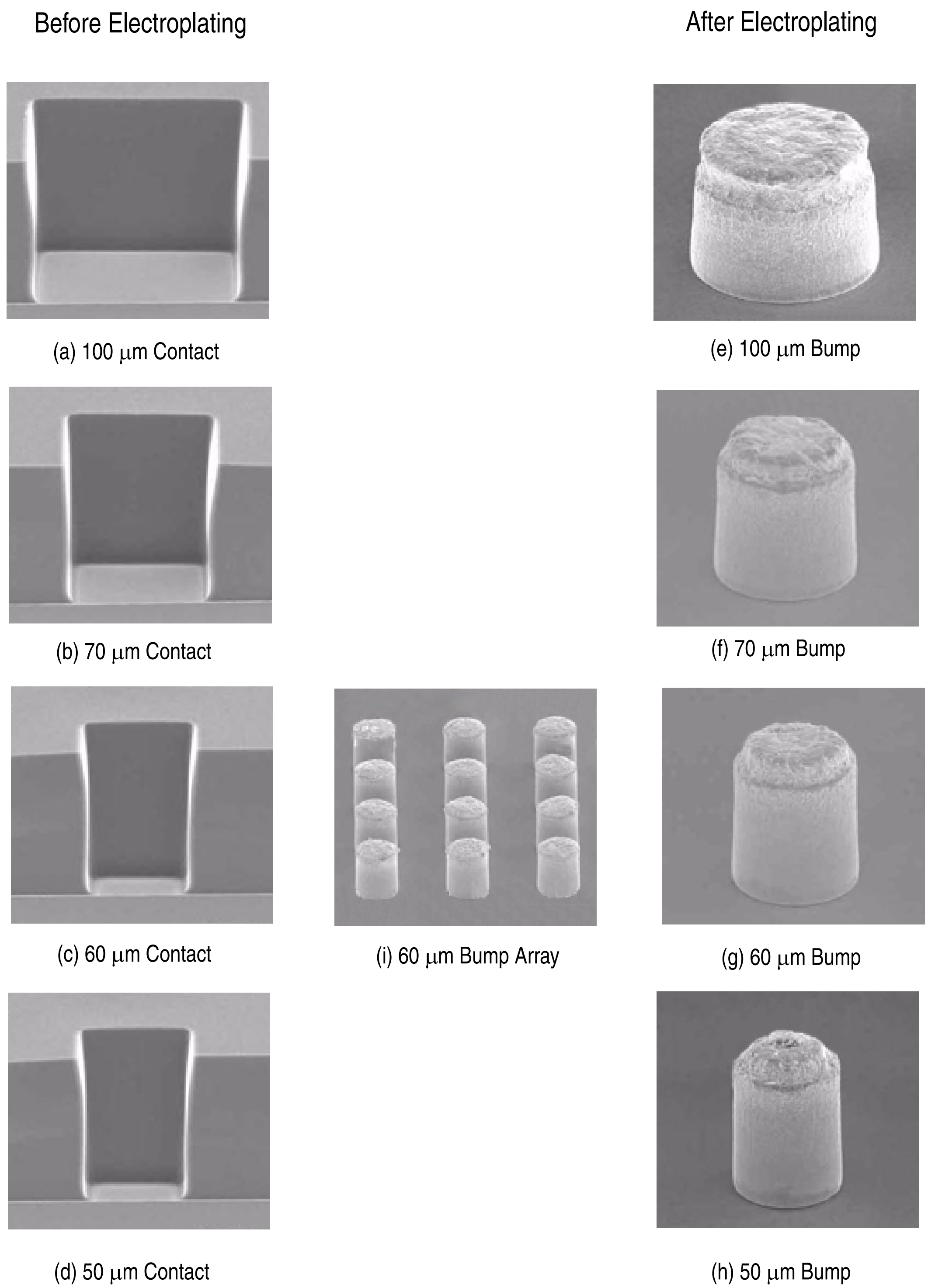

Figure 7: SEM Photographs illustrating the CD linearity of 100 µm thick Shin-Etsu SIPR 7120 before and after electroplating. The photoresist images are a square contacts and the electroplated structures are round solder bumps. The exposure conditions are ghi-line exposure, -20 µm focus, 5800 mJ/cm^2.